Amendments to the Specification

Paragraph at page 9, line 25 to page 10, line 11:

The control system is a completely digital system based on a microprocessor 150 operating at a clock rate, approximately 25.6MHz in the embodiment to be described later in detail, set by an oscillator 152. ~~other~~ Other types of microcontrollers may also be utilized. Preferably, the microprocessor 150 and oscillator 152 together with the assembled ESA array 140 and driver integrated circuit 144 and perhaps a separate low-voltage control integrated circuit are mounted on a standard substrate carrier, typically formed of plastic or ceramic, with a small number of wire bonds connecting the microprocessor 150 and the periphery of the driver chip 146. The microprocessor 150 receives commands SYSTEM COMMAND from the system controlling the optical switch and through multiplexing controls a large number of actuator cells through a small number of control lines CLK, CE*, DATA, ROW/COL, and WE*. These commands include most importantly the desired positions of the mirrors 142, which effect switching between optical ports of the system. For the 12×40 mirror array discussed above, each mirror needs to be positionable in the major direction at, for example, six gross tilt angles as well as at finer angular resolution corresponding to tuning around those positions and in the minor direction in a fine resolution providing power tuning. As a result, two actuators are required for each mirror 142. It is understood that the invention can be applied to a different number of MEMS elements and is not limited to two-axis tilting.

Paragraph at page 11, line 23 to page 12, line 5:

The microprocessor 150 controls a time multiplexed storage of position control in the actuator array ASIC 144. In the pulse width modulation control, the position control is dictated by a multi-bit duty cycle. The position data DATA and a row and column address ROW/COL for which the data DATA is to be applied are delivered to the actuator array 144 by the microprocessor 150. A write enable signal WE or its complement WE* causes the addressed cell

of the actuator array 144 to store the position data DATA. Thereby, all cells are sequentially stored with position data DATA, and the position data DATA of any one cell can be updated as desired. A compare enable signal CE or its complement CE* from microprocessor causes all of the cells in the actuator array to be simultaneously PWM controlled according to position data stored in the respective cell with a timing referenced to a clock signal CLK supplied from the microprocessor 150 as derived from an oscillator 152. In the described example, the electrostatic microactuators are subjected to a bipolar signal oscillating at 50kHz and the CLK signal is 512 times greater, that is, 25.6MHz.

Paragraph at page 16, lines 1-11:

The control logic may be implemented in a number of ways, but an architecture, ~~show~~ shown in FIG. 7, based on content-addressable memory (CAM), has been found to be particularly advantageous in producing waveforms illustrated in FIG. 6. A 9-bit counter 220 is driven by a clock signal CLK at a frequency 512 times the drive frequency f_{DRIVE}, that is, at 25.6MHz in the example design. The counter outputs R_0-R_8 are applied to all CAM cells to be described later. The most-significant bit R_8 is used as a polarity indicator in creating the bipolar drive signal. A high-voltage driver 221 level-shifts the most-significant bit R_8 to create the oscillating binary common node signal V_C that is commonly supplied to all actuators or some plurality of them, for instance, those in a quadrant of the array to be described later. Thus, R_8 and V_C are synchronized. The high-voltage amplifer 221 may be implemented with a structure similar to the push-pull transistors 195, 198 and level shifter 202 of FIG. 5.

Two Paragraphs at page 16, line 22 to page 17, line 11:

The logic implemented by the CAM circuitry can be understood with reference to the block diagram of FIG. 7. [[A]] The 9-bit reference counter 220 is clocked by [[a]] the square wave clock signal CLK, for example at 25.6MHz, which for the rest of the circuit is a complemented compare enable CE*. Only one counter 220 is needed for the array, but if the

array is ~~physical~~ physically separated into ~~subarray~~ subarrays, these can be ~~drivent~~ driven independently by independent counters. The rest of the circuitry for the most part needs to be replicated for each logic cell, that is, one for each microactuator. However, some high order address decoding may be shared.

Each logic cell is connected to the microprocessor 150 by a number of lines shared in common by all the logic cells and constituting a microprocessor interface MICROPROCESSOR INTERFACE. An 8-bit latch 222 receives four data lines D_7-D_0 from the microprocessor that carry the 8-bit duty cycle DUTY FACTOR intended for that cell. A programmed address decoder 224 receives four bits A_3-A_0 of row address ROW ADDR and five bits A_8-A_4 of column address COLUMN ADDR. The address decoder 224 is permanently programmed with a unique 9-bit address The address decoder 224 receives as a write enable signal WRITE ENABLE a complemented write enable signal WE*. When WE* goes true, the decoder 224 compares its stored address with the address on the address lines A_8-A_0. If the two agree, the address decoder 222 outputs a latch signal to the 8-bit latch 222 to latch the duty factor value DUTY FACTOR currently on the data lines D_7-D_0. The operations described to this point are performed in an operation to initialize or to update position information for a particular actuator cell. Once the duty cycle data DUTY FACTOR is latched, that value is used for that cell until the locally stored data is updated.

Paragraph at page 17, line 20 to page 18, line 3:

An example of the physical layout of the combined high-voltage and low-voltage chip is illustrated in plan view in FIG. 8. The 24×40 driver array 146, used for two-axis control of a 12×40 mirror array, is divided into four array quadrants, each having 20 columns of drivers, vertically extending in the illustration, and 12 rows of drivers. Positioned on opposed sides of the driver array 146 is control circuitry similarly divided into four quadrants. Each quadrant contains a row 230 of column decoders, a row 232 of row decoders, and a row 234 of content addressable memory (CAM) registers. A CAM register, which will be described in much detail later, acts as a multi-bit comparator with written and stored values serving as two sets of inputs to

the comparator. The circuitry within these rows 230, 232, 234 is replicated in logic columns 236, further illustrated in the plan view of FIG. 9, controlling six pairs 238 of high-voltage driver cells for the major axis control MAJOR and minor axis control MINOR of the mirrors. Only one column decoder is required for the high-order address of each logic column 236, but 12 row decoders and 12 CAM registers are required for all the 12 actuator cells controlled by the logic column 236.

Paragraph at page 23, line 22 to page 24, line 4:

Although the CAM register is particularly advantageous for implementing the block diagram of FIG. [[6]] 7, other implementations are possible. For example, a control logic utilizing commonly available logic circuits is illustrated in the block diagram of FIG. 16. A column enable signal CE propagates to all logic cells in the column direction, and a row enable signal RE propagates to all logic cells in the row direction. All cells receive a load signal LD, an n-bit data signal D, a common clock signal COMCLK at the frequency of the actuator signal, e.g., 50kHZ, and a master clock signal MCLK, which is the product of the COMCLK signal and twice the resolution of the pulse width modulation, e.g., 25.6MHz. The following circuitry is associated with each logic cell. Storing of the pulse width value is triggered by an AND gate 360 receiving on its input the load signal LD, the row enable signal RE, and the column enable signal CE. The output RESET of the AND gate 360 is connected to the reset or LDR input of a n-bit register 362 causing it to latch the current *n* bits of data D indicating the desired pulse width.